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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,651	06/25/2001	Masahiro Nagata	6340-000018	5516

27572 7590 03/14/2005

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,651	NAGATA, MASAHIRO	
	Examiner	Art Unit	
	Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3-15* is/are allowed.

6)☒ Claim(s) *2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to amendment received on December 14, 2004. Claims 1-15 are pending.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Charles et al., U. S. Patent 5,790,842.

Per claim 2:

A) Charles et al teach the following claimed items:

1. a control processor operating according to a high speed clock (40.5 MHz) obtained by multiplying (1.5x27MHz) a standard clock (27 MHz) with ASIC 20 of figures 1 and 6A and at column 18, lines 41-67;

2. input means with flip-flop 260 of figure 6A;

3. output means with flip-flop 272 of figure 6A;

4. performing an operation (state based logic operation) according to a value of signal information (YUV27IN) captured from the input means synchronously with the standard clock (27 MHz) and changing a value (YUV27OUT) of the output means (flip-flop 272) by the control processor synchronously with the standard clock within a predetermined number of cycles of the standard clock with figures 6A and 6B and at column 20, lines 7-67.

4. Applicant's arguments filed on December 14, 2004 have been fully considered but they are not persuasive.

In the Remarks, applicant has argued in substance that:

A. Charles et al do not show, teach or suggest performing an operation (state based logic operation) according to a value of signal information captured from the input means synchronously with the standard clock (27 MHz) and changing a value of the output means (flip-flop 272) by the control processor synchronously with the standard clock within a predetermined number of cycles of the standard clock.

B. The state-based logic does not change a value that is output by the state-based logic synchronously with the first clock and within a predetermined number of cycles of the first clock.

C. Since the second clock is a non-integer multiple of the first clock, the signals output by the state-based logic may only be synchronous with the first clock when the cycle number is evenly divisible by the ratio between the second clock and the first clock. Applicant's high speed clock is an integer multiple of the standard clock. Therefore, the control processor is capable of generating the output signal within a predetermined number of cycles of the standard clock.

5. As to point A, the examiner disagrees with applicant's contentions. Charles clearly show and teach performing an operation (state based logic operation) according to a value of signal information (YUV27IN) captured from the input means synchronously with the standard clock (27 MHz) and changing a value (YUV27OUT) of the output means (flip-flop 272) by the control processor synchronously with the standard clock within a predetermined number of cycles of the standard clock as

described in the above rejection. Charles shows that output value YUV27OUT is changed within a predetermined number of cycles of standard clock 27 with figure 6B.

As to point B, the above rejection shows that the examiner pointed to flip-flop 272 of figure 6A as the output means not state-based logic 266. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the detailed description of Charles state-based logic) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant seems to be arguing that Charles is different from claim 2 because Charles describes details of his processing circuitry that are not recited in claim 2. Applicant is clearly arguing how the details of Charles differ from the claim rather than arguing how the language of the claim differs from Charles as required under rule 1.111(b). Claim 2 does not recite a state-based logic element. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

As to point C, regarding the high speed clock being an integer multiple of the standard clock, it is noted that the features upon which applicant relies (i.e., the integer multiple) are not recited in the rejected claim and can not be read into the claim. In addition, the examiner disagrees with applicant's contention that the state-based logic does not change a value that is output by the state-based logic synchronously with the

first clock within a predetermined number of cycles of the first clock because the second clock is a non-integer multiple of the first clock. Figure 6B shows that the rising edges of the first and second clocks are synchronized (aligned) every two cycles of the slow clock (27) and/or are aligned every three cycles of the fast clock (40.5). In addition, Charles describes that the circuitry of figure 6A was designed to operate based on the non-integer clock ratio and can transfer signals between the two clock frequency domains at column 18, lines 50-67 and at column 20, lines 7-57. Furthermore, figure 6B clearly shows that the output value YUV27OUT is changed within a predetermined number of cycles of the standard clock (27) from the cycle when the input signal YUV27IN is captured. Charles also describes that it is known to use an integer multiple clock at column 18, lines 55-63. The non-integer multiple clock does not preclude the output value YUV27OUT from being changed within a predetermined number of cycles of the standard clock (27 MHz).

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler
Primary Examiner
Art Unit 2115